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D. Remarks

Objections to Drawings

Proposed amended drawings are included herein. FIGS. 8A, 8B and 8C have been amended to include the label "BACKGROUND ART".

Rejection of Claims 1-20 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,878,051 (*Sharma et al.*).

The rejection of claims 1-10 will first be addressed.

The invention of claim 1 is directed to a programmable logic device assembly. The programmable logic device assembly includes a programmable logic circuit that provides functions according to configuration data including a self-test function. The assembly further includes at least one nonvolatile store of the programmable logic device assembly coupled to the programmable logic circuit. The nonvolatile store provides self-test configuration data for the programmable logic circuit and can subsequently store user configuration data.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. Because the reference *Sharma et al.* does not show all elements of claim 1, this ground of rejection is traversed.

The cited reference *Sharma et al.* does not show or suggest a programmable logic circuit that provides a self-test function. Nor does the cited reference show a nonvolatile store that provides self-test configuration data for the programmable logic circuit. Instead, *Sharma et al.* teaches field-programmable gate array (FPGA) that can configured to test other devices, and not for a self-test of the FPGA.

In more detail, *Sharma et al.* shows an assemblage that includes an FPGA connected to a various devices, which can include a static random access memory (SRAM), read-only-memory (ROM), first-in-first-out memory (FIFO), adder, multiplier, application specific integrated circuit (ASIC), and a processor. The FPGA (argued to correspond to Applicant's programmable logic circuit) can be configured to be a special purpose tester for these various devices and not for a self-test, as recited in claim 1:

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> [T]he field-programmable gate array 40 is reconfigurable in response the test bus signals, to form... a special-purpose tester for any one of the SRAM 14, ROM 16, FIFO 17, adder 18, multiplier 20, ASIC 21, or for any other functionality...[1]

Thus, while the FPGA of *Sharma et al.* may be configured as a tester for various devices, it is clear it does not provide self-test function, and is never provided with self-test configuration data.

Sharma et al. teaches that configuration data can be stored in an on board memory, but such configuration data is not for a self test of the FPGA, but rather for a self-test of the other devices:

> [T]he configuration information required for the ordinary operating state of FPGA, for the *memory self-test state*, for the *FIFO self-test state*, and for the *self-test states of the FPGA 40 as required for testing any known device 14-21*... Those skilled in the art know that the configuration information could also be stored on-board the assemblage in some form of ROM, such as a UV-erasable ROM, or in nonvolatile RAM.[2]

The above excerpt is believed to clearly show that the FPGA of *Sharma et al.* can provide a memory self-test, FIFO self-test, ROM self-test etc., but never shows or suggest an FPGA self-test.

Applicant notes that claim 1 recites a programmable logic circuit that provides functions including a self-test function. Applicant believes the term "self-test" is well understood in the art to not include the testing of some other device. Nonetheless, to support a fair reading of claim 1 (particularly in light of the Specification) Applicant's provide the following well-accepted definition:

> **self-test**... A test or series of tests, performed by a device *upon itself*...[3]

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[1] *Sharma et al.*, Col. 4, Lines 43-48.
[2] *Sharma et al.*, Col. 6, Lines 38-46.
[3] The Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, IEEE Press, 2000, Page 1021, emphasis added.

In light of all of the above, it is believed the cited reference *Sharma et al.* never shows or suggests a programmable logic circuit that provides a function including a self-test, nor a nonvolatile store that provides self-test data for the programmable logic circuit.

Various claims depending from claim 1 include additional limitations not shown in the cited reference.

Claim 8 recites that the at least one nonvolatile store includes a mask programmable ROM that stores self-test configuration data, and a separate nonvolatile memory that can store user configuration data. As noted above, *Sharma et al.* shows a ROM (that is, one nonvolatile memory) that stores all configuration data for the FPGA. The reference never teaches separate nonvolatile memories for self-test configuration data and user configuration data. Accordingly, the reference does not show all limitations of claim 8.

Claim 9 recites that the at least one nonvolatile store includes at least two sectors, and self-test configuration data is stored in a first sector. Claim 10 further specifies that the first sector is a boot sector. Such limitations are not shown in *Sharma et al.* Applicant respectfully request a citation as to where separate sectors storing such configuration are shown in the reference. Accordingly, because the reference does not show all limitations of claims 9 or 10, the rejection of claims 9 and 10 is traversed for this additional reason.

For all of these reasons, this ground for rejection is traversed.

The rejection of claims 11-17 will now be addressed.

The invention of claim 11 is directed to a method that includes performing a self-test on a programmable logic circuit of one package according to self-test configuration data in a self-test nonvolatile store of the one package. The method further includes storing user configuration data in a user nonvolatile store if the programmable logic circuit passes the self-test.

To address this ground for rejection, Applicant incorporates by reference herein the same general comments set forth above for claim 1. Namely, that while *Sharma et al.* shows an FPGA (argued to correspond to Applicant's programmable logic circuit), the reference never shows or suggests a self-test on such an FPGA.

Accordingly, *Sharma et al.* does not show all the limitations of claim 11, and this ground for rejection is traversed.

Claim 13, which depends from claim 11, includes additional limitations not shown in the cited reference.

Claim 13 recites that the step of storing user configuration data includes the particular limitations of programming user configuration in locations that store self-test configuration data. Such a limitation is not shown in *Sharma et al.* As noted above, *Sharma et al.* teaches that some form of ROM can be provided to store configuration data for the FGPA, but never teaches programming user configuration data in locations that store self-configuration data.

For this additional reason, the rejection of claim 13 is traversed.

The rejection of claims 18-20 will now be addressed.

Claim 18 is directed to a programmable logic assembly self-test method. The method includes the steps of storing self-test information in a first nonvolatile store of the assembly that places a programmable logic circuit of the assembly into a self-test configuration, executing a self-test on the programmable logic circuit, and providing user configuration information that places the programmable logic circuit in a user configuration.

To address this ground for rejection, Applicant incorporates by reference the same general comments set forth above for claims 1 and 11. Namely, that *Sharma et al.* never shows or suggests a self-test on the FPGA (argued to correspond to Applicant's programmable logic circuit).

Accordingly, *Sharma et al.* does not show all the limitations of claim 18, and this ground for rejection is traversed.

Claim 20, which depends from claim 18, recites that user configuration data is stored in a second nonvolatile stores which is different than that first nonvolatile store (which stores the self-test information). To address the rejection of this claim, Applicant's incorporate by reference the comments set forth above for claim 8.

For all of these reasons this ground for rejection is traversed.

Rejection of Claims 1-20 Under 35 U.S.C. §102(b) based on Applicant's Background Art.

An apparent additional anticipation rejection was raised in the current Office Action:

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> Examiner also notes that Applicant's admitted prior art Figs. 8a-c anticipate claims 1-20 since claims 1-20 depicted by Figs. 2a-c are merely relocating simple elements of the admitted prior art Figs. 8a-c. It has been held that mere relocation of parts of an invention involves only routine skill in the art. *In re Japiske*, USPQ 70.[4]

This ground for rejection is improper, and should be withdrawn.

First, the rejection appears to indicate that Figs. 2a-c depict Applicant's claims 1-20. This is improper. Applicant's claim language represents the metes and bounds for which patent protection is being sought, not one particular embodiment of Applicant's invention. That is, a prior art reference can only anticipate Applicant's claims, not Applicant's drawings.

Second, the rationale relied upon is unrelated to anticipation. In re Japiske, is directed to rationales to support obviousness rejections. Thus, the rationale relied upon cannot support an anticipation rejection. That is, if an invention consisted of the relocation of elements shown in a reference, the invention could not be anticipated by the reference, as such elements would not be "arranged as in the claim". However, as held in In re Japiske, such a relocation of elements might be an obvious variation of a prior art teaching.

Third, FIGS. 8A to 8C do not show a relocation of simple elements as the two figures do show different elements. The PLD 204 of FIGS. 8A to 8C includes area dedicated to BIST circuits 804-1. One of the advantages of the embodiment of FIGS. 2A to 2C is that such dedicated circuitry can be reduced or eliminated.[5] In addition, the NV MEMORY of FIGS. 8A to 8C does not receive BIST DATA. Still further, the NV MEMORY of FIGS. 8A to 8C does not provide BIST DATA.

For all of these reasons, this ground of rejection is improper and should be withdrawn.

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[4] See the Office Action, dated 10/09/2003, Page 5, Lines 10-13.
[5] See Applicant's Specification, Page 11, Lines 1-5.

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The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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